REMARKS

Claims 1-11, 26, 28-30, and 32-39 are pending in the application. Claims 1, 8, 26, 30, 33, and 37 are independent. By the foregoing Amendment, claims 1, 8, 26, 30, 33, and 37 have been amended. These changes are believed to introduce no new matter and their entry is respectfully requested.

Rejection of Claims 1-2, 4, 26, and 29-30 Under 35 U.S.C. §103(a)

In paragraph 3 of the Office Action, the Examiner rejected claims 1-2, 4, 26, and 29-30 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,231,314 to Andrews (hereinafter "Andrews") in view of U.S. Patent No. 6,310,571 B1 to Yang et al. ("hereinafter "Yang").

To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. (MPEP §2143.) Applicant respectfully traverses the rejection.

Amended independent claims 1 and 26 recite in pertinent part "an integrated circuit having circuitry ***to test input levels of the integrated circuit***, the circuitry to test the input levels" (emphasis added). Amended claim 30 recites in pertinent part "***testing input levels*** of at least one integrated circuit device" (emphasis added).Support for these changes can be found in Applicant's Specification at page 5, line 15 according to at least one embodiment of the invention.

Andrews appears to be directed to testing the timing of an integrated circuit rather than testing input levels of an integrated circuit and Yang appears to be directed to an analog-to-digital converter (ADC) for an image sensor or digital pixel sensor. Applicant respectfully submits that Andrews and Yang, individually or in combination, fail to teach an integrated circuit having circuitry to test input levels of the integrated circuit as recited in the amended independent claims and that nowhere in Andrews or Yang is testing input levels of an integrated circuit mentioned. Therefore, Andrews in view of Yang fail to teach or suggest each and every

element of the claimed invention. Accordingly, Applicant respectfully submits that claims 1, 26, and 30 are patentable of Andrews in view of Yang. Claims 2, 4, and 29 properly depend from claims 1 or 26, which applicants respectfully submit are patentable. Accordingly, Applicant respectfully submits that claims 2, 4, and 29 are patentable as well. MPEP §2143.03 provides that if an independent claim is unobvious, then any claim depending from the independent claim is unobvious (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Applicant therefore respectfully requests that the Examiner reconsider and remove the rejections to claims 1-2, 4, 26, and 29-30.

Rejection of Claims 3, 5-6, and 28 Under 35 U.S.C. §103(a)

In paragraph 4, the Examiner rejected claims 3, 5-6, and 28 under 35 U.S.C. §103(a) as unpatentable over Andrews in view Yang in further view of U.S. Patent No 6,085,345 to Taylor (hereinafter "Taylor"). Applicant respectfully traverses the rejection.

Claims 3 and 5-6 properly depend from claim 1, and claim 28 properly depends from claim 26, which applicants respectfully submit are patentable. Accordingly, Applicant respectfully submits that claims 3, 5-6, and 28 are patentable as well. See MPEP §2143.03 (citing *In re Fine*). Applicant therefore respectfully requests that the Examiner reconsider and remove the rejections to claims 3, 5-6, and 28.

Rejection of Claims 7 and 40-43 Under 35 U.S.C. §103(a)

In paragraph 5, the Examiner rejected claims 7 and 40-43 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of Taylor in further view of U.S. Patent No 6,477,674 to Bates et al. (hereinafter "Bates") in further view of Yang. Applicant respectfully traverses the rejection.

Claim 7 properly depends from claim 1, which applicants respectfully submit is patentable. Accordingly, Applicant respectfully submits that claim 7 is patentable as well. See MPEP §2143.03 (citing *In re Fine*). Claims 40-43 were canceled in a previous Paper, which cancellation renders the rejection moot. Applicant therefore respectfully requests that the Examiner reconsider and remove the rejections to claims 7 and 40-43.

Rejection of Claims 8-11, 32, and 37-38 Under 35 U.S.C. §103(a)

In paragraph 6, the Examiner rejected claims 8-11, 32, and 37-38 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of Taylor. Applicant respectfully traverses the rejection.

Amended independent claims 8 and 37 recite in pertinent part "an integrated circuit having circuitry ***to test input levels of the integrated circuit***, the circuitry to test the input levels" (emphasis added). Amended claim 30 recites in pertinent part "***testing input levels*** of at least one integrated circuit device" (emphasis added).Support for these changes can be found in Applicant's Specification at page 5, line 15 according to at least one embodiment of the invention.

Both Andrews and Taylor appear to be directed to testing the timing of an integrated circuit. The Examiner asserts that Taylor teaches "determine a set of trip points for the sent of sense amplifiers" and "testing of levels." But, Applicant respectfully submits, Taylor fails to teach "testing input levels" as defined in Applicant's Specification. For example, Applicant's Specification at page 1, lines 17-26 describe that "[p]roduct manufacturers perform certain tests on the devices in order to guarantee the product complies with the specifications. For example, when the DC specifications state that the "input low voltage" (VIL) is three hundred millivolts at a minimum and eight hundred millivolts at a maximum, the manufacturer has tested the product to ensure that a DC voltage between three hundred millivolts and eight hundred millivolts applied to the part is interpreted as a logical "zero." Similarly, when the DC specifications state that the "input high voltage" (VIH) is two volts at a minimum and the supply voltage (V_{CC}) at a maximum, the manufacturer has tested the part to ensure that a DC voltage between two volts and Vcc applied to the part is interpreted as a logical 'one.'" Applicant respectfully submits that this is what is meant by the term "input levels testing."

With this in mind, Applicant respectfully submits that Taylor does not teach "testing input levels" as recited in claims 8 and 37 and given light in Applicant's Specification. Andrews also fails to teach, as the Examiner does not assert, testing input levels. This is because Andrews

and Taylor are not concerned with the DC specifications for an integrated circuit, but with timing. Thus, Andrews and Taylor, individually or in combination, fail to teach each and every element of the claimed invention and Applicant respectfully submits therefore that claims 8 and 37 are patentable of Andrews in view of Taylor. Claims 9-11 properly depend from claim 37, claim 32 properly depends from claim 30, and claim 38 properly depends from claim 37. Accordingly, Applicant respectfully submits that claims 9-11, 32, and 37 are patentable as well. See MPEP §2143.03 (citing *In re Fine*). Applicant therefore respectfully requests that the Examiner reconsider and remove the rejections to claims 8-11, 32, and 37-38.

Rejection of Claims 33-36 and 39 Under 35 U.S.C. §103(a)

In paragraph 8, the Examiner rejected claims 33-36 and 39 under 35 U.S.C. §103(a) as unpatentable over Andrews in view of Taylor in further view of Bates. Applicant respectfully traverses the rejection.

Amended independent claim 33 recites in pertinent part "an integrated circuit having circuitry ***to test input levels of the integrated circuit***, the circuitry to test the input levels" (emphasis added). Support for these changes can be found in Applicant's Specification at page 5, line 15 according to at least one embodiment of the invention.

As discussed above with reference to claims 8 and 37, Applicant respectfully submits that Andrews in view Taylor does not teach "testing input levels" as recited in claim 33 and given light in Applicant's Specification and Bates does not make up for the deficiency. Again, this is this is because Andrews, Taylor, and Bates all appear to be directed to testing the timing of an integrated circuit. They are not concerned with the DC specifications for an integrated circuit. Thus, Andrews, Taylor, and Bates, individually or in combination, fail to teach each and every element of the claimed invention and Applicant respectfully submits therefore that claim 33 is patentable of Andrews in view of Taylor in further view of Bates Claims 34-36 properly depend from claim 33 and claim 39 properly depends from claim 37, which as Applicant discussed above is patentable over the art of record. Accordingly, Applicant respectfully submits that claims 34-36 and 39 are patentable as well. See MPEP §2143.03 (citing *In re Fine*). Applicant

therefore respectfully requests that the Examiner reconsider and remove the rejections to claims 33-36 and 39.

CONCLUSION

Applicant submits that all grounds for rejection have been properly traversed, accommodated, or rendered moot and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 8/25/2005

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